Sub B1

IN THE CLAIMS

1. (Amended) A memory system that receives addresses corresponding to data in an order comprising:

A1

an address buffer that receives addresses in said order;

a memory array;

a control circuit that selects a memory reference from a set of pending memory references in said address buffer to present to the memory array, said references being presented to said memory array in an order different than the order in which they were received; and

a read buffer, that receives data read out from the memory array.

Sub B1

A3

13. (Amended) A method of accessing memory comprising the steps of:

receiving a sequential plurality of memory access requests in the form of an address inputs;

buffering the plurality of address inputs;

initiating an out of order memory access request to a memory array for one of the sequential plurality of memory access requests such that one of the plurality of address inputs is requested in an order different than the order in which the one address was received;

selecting a memory reference from among a set of pending memory references and presenting this memory reference to said memory array; and

buffering read results of those memory access requests corresponding to read operations.